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Influence of Interface Morphology on Hysteresis in Vapor-Deposited Perovskite Solar Cells

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Metal halide perovskite materials show great promise for photovoltaic devices, with power conversion efficiencies (PCE) based on this class of materials having recently exceeded 22%.[1] However, organic-inorganic perovskite photovoltaic devices have been beset by anomalous hysteresis, whereby the current–voltage (*J–V*) characteristics are dependent upon both scan rate and direction.[2] Furthermore, discrepancies have been reported between the initial measured solar cell efficiency and measurements taken after holding the device at a sustained bias over a period of time.[3–5] Both ion migration in the bulk of the thin film and charge trapping at the perovskite surface have been proposed as causes of the anomalous hysteresis.[6–8] In this systematic study we use a single batch of vapor-deposited $CH_3NH_3PbI_3$ ($MAPbI_3$) on a range of device architectures to show that the cause of hysteresis in planar heterojunction $MAPbI_3$ solar cells originates from the interface between the perovskite and the electron transport layer, and that interface engineering can be used to eliminate hysteresis in these devices. Furthermore, we show using transmission electron microscopy (TEM) and scanning transmission electron microscopy (STEM) that under identical growth conditions the interface affects perovskite morphology and crystallinity. We link devices incorporating amorphous regions of $MAPbI_3$ at the perovskite-electron transport layer (ETL) interface, with hysteresis and poor stabilized performance of solar cell devices.

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The perovskite methylammonium lead triiodide ($MAPbI_3$) has been intensively studied since its initial breakthrough as a photoabsorber.[9] It has been shown to possess material properties ideally suited for photovoltaic devices such as a high absorption coefficient, long electron–hole diffusion lengths,[10] high-charge carrier mobilities,[11] and a favorable bandgap of ≈1.6 eV.[12,13] Organic–inorganic metal halide perovskite materials can be processed by a diverse range of deposition techniques and on a variety of substrates.[14–17] Solution coating techniques and vapor deposition are the two key approaches that have produced highly efficient solar cells.[18,19] Dual source vapor deposition was used to create the earliest high-efficiency planar heterojunction perovskite solar cell using an $MAPbI_{3-x}Cl_x$ perovskite.[20] Solution processing techniques have been used to further explore the planar heterojunction device architecture by changing both the charge transport layers and the perovskite photoactive layer.[21,22] However, planar heterojunction solar cells based on both vapor-deposited and solution-processed $MAPbI_3$ have been reported to exhibit significant hysteresis in their *J–V* characteristics.[2–4]

In this study we focus on vapor-deposited perovskite solar cells, as vapor deposition allows us to deposit a perovskite film simultaneously on multiple devices with different planar architectures under identical conditions. Vapor deposition involves heating precursor solids in high vacuum, allowing the sublimed material to uniformly condense on the substrate.[23] While vapor deposition is currently less commonly used compared with solution processing, it considerably reduces the amount of independent variables, leading to highly uniform and pinhole-free thin films on a consistent basis.[20] As a technique widely used in industry for organic light emitting diodes and inorganic semiconductors, thermal vapor deposition has also been shown to have a high rate of batch-to-batch reproducibility.[24] There are two main methods to create an $MAPbI_3$ thin film by thermal vapor deposition: co-evaporation, by which the precursor materials methyl ammonium iodide and lead iodide (PbI_2) are evaporated simultaneously[25] and a two-step evaporation, whereby the precursors are deposited sequentially.[17] In this study, we focus on films produced by dual source thermal co-evaporation.

To establish a link between device *J–V* hysteresis and architecture we first present statistics from 186 planar heterojunction solar cells produced from 17 deposition batches, where deposition parameters and annealing conditions were optimized for the particular architecture. In order to understand the underlying cause of hysteresis we will then concentrate on a subset of architectures where the perovskite was deposited in the same vapor deposition run, without any post-deposition thermal annealing.

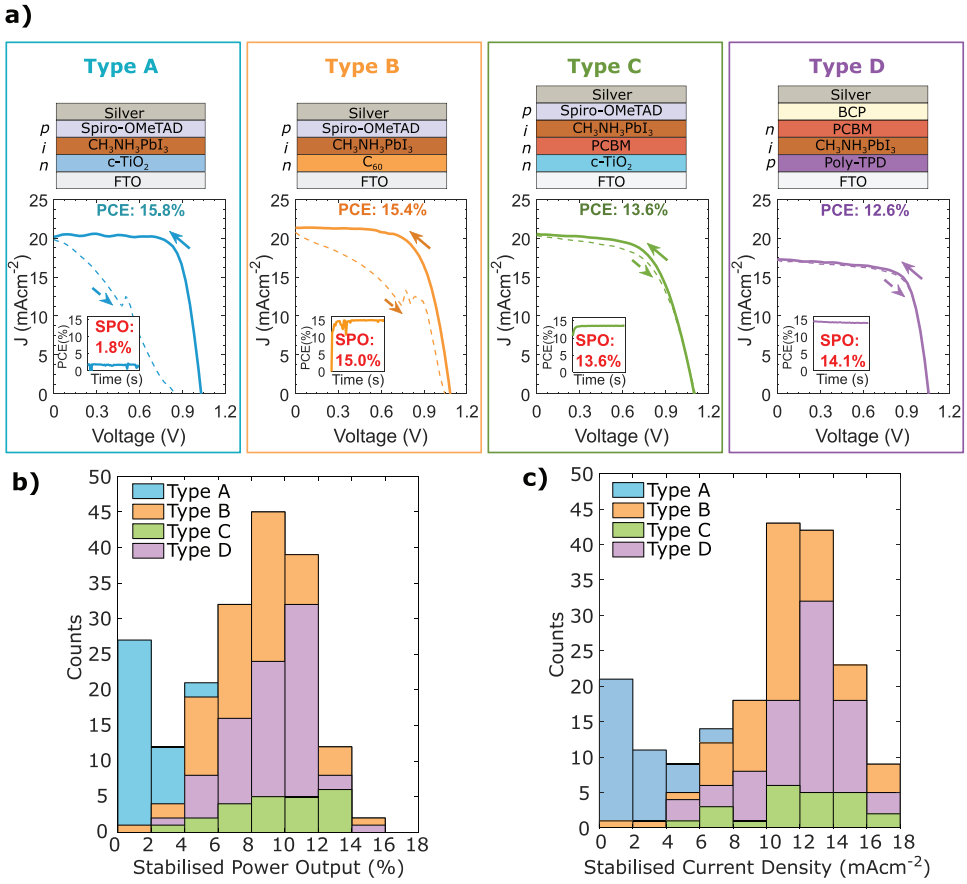

Figure 1. a) Schematics for different planar heterojunction device architectures with varying n-type layers (type A–C) and an inverted device architecture (type D), with the corresponding current–voltage (*J–V*) curves for the champion devices. The arrows denote the scan direction of the *J–V* sweep. The inset in each *J–V* curve shows the stabilized power output (SPO) after 50 s under a constant bias. Histograms showing the statistical variation for the different device types. b) Stabilized power output (SPO). c) Stabilized current density (J_{mpp}). Type A devices (blue) have very poor stabilized currents and efficiencies compared to devices which use n-type layers used in the device types B (orange), C (green), and D (purple). Type B devices show hysteresis, yet the stabilized device parameters are significantly higher compared to type A devices. Evaporation conditions were individually optimized for each device architecture; detailed information on layer thicknesses and fabrication methods can be found in the Supporting Information.

A clear link between *J–V* hysteresis and device architecture can be seen by examining **Figure 1** which summarizes the performance of 186 devices with four common device architectures labeled A–D. For types A–C the $MAPbI_3$ perovskite layer was evaporated onto an ETL, a geometry that is common for most published perovskite solar cells and which we will refer to as a "regular" device architecture.[26] The ETLs for types A, B, and C were TiO_2, C_{60}, [6,6]-phenyl C_{61} butyric acid methyl ester (PCBM), respectively, while the hole transport layer (HTL) was 2,2′,7,7′-tetrakis-(*N*,*N*-di-4-methoxyphenylamino)-9,9′-spirobifluorene (Spiro-OMeTAD). In contrast, for the type D, which we will refer to as an "inverted" device architecture, the PCBM ETL was deposited after the $MAPbI_3$ was evaporated on a poly(4-butylphenyl-diphenyl-amine) HTL.[27]

Figure 1a shows the *J–V* characteristics of the champion devices for each architecture type A–D. For the type A (c-TiO_2 ETL) a clear hysteresis can be seen between the forward and reverse *J–V* sweep. While the standard method to determine the PCE of a solar cell is based on analysis of the *J–V* curve,[28] it has been proposed that an alternate method measuring the "stabilized power output" (SPO) may be more appropriate in assessing the working efficiency of hysteretic cells.[2] In this method PCE is measured as a function of time, by holding the device at a load corresponding to the maximum power point. Maintaining the device at constant bias more closely simulates the operation of a solar cell under load, thus measurements of SPO and stabilized current density at maximum power point (J_{mpp}) can be more representative indicators of the true device efficiency.

The type A device utilizes the wide bandgap semiconductor compact TiO_2 (c-TiO_2). It has been implemented in metal halide perovskite devices as an ETL, largely due to its historic use in dye-sensitized solar cells.[29] The type A device represented in Figure 1a shows a PCE (measured by reverse *J–V* sweep) of 15.8%, which is an order of magnitude higher than the SPO (1.8%). In fact, all c-TiO_2 devices tested under a constant bias showed significantly lower SPO (<6%) and J_{mpp} (<8 mA cm^{-2}) as shown by the statistics in Figure 1b,c (blue columns).

Device architectures, B and C, show a good agreement between the PCE and SPO. Interestingly for the type B device, in which the c-TiO_2 ETL was entirely replaced by C_{60}, there is significant *J–V* hysteresis yet a good agreement between PCE (15.4%) and SPO (15.0%). Type C devices, which incorporate a

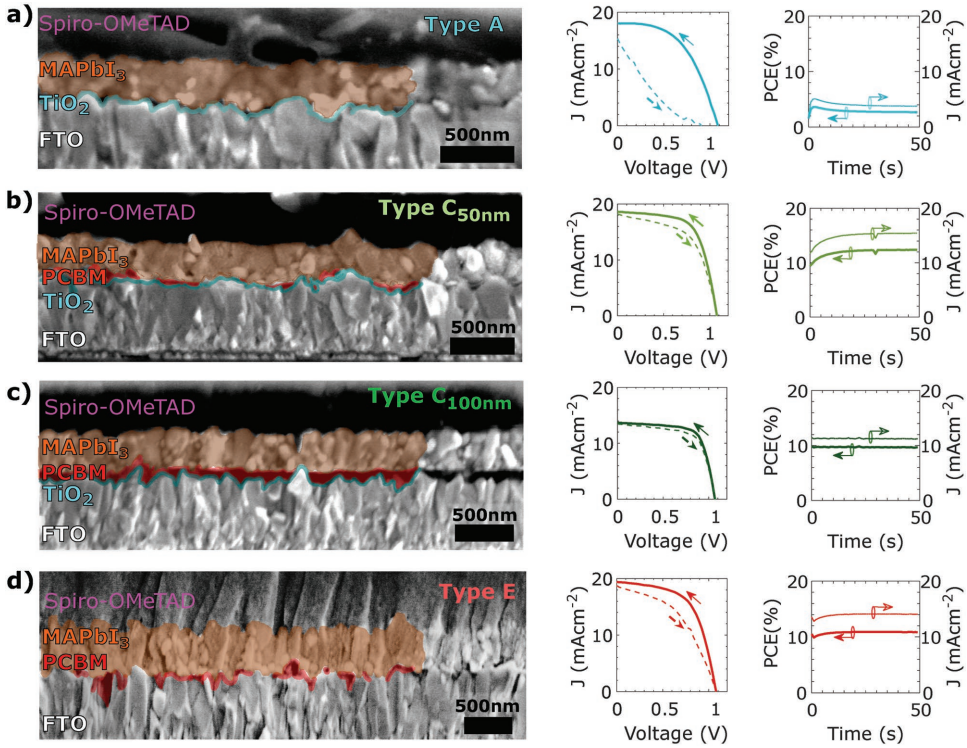

Figure 2. SEM images, *J–V* curves, and stabilized power output over 50 s of operation for a) Type A, b) Type $C_{50\ nm}$, c) Type $C_{100\ nm}$, and d) Type E. Devices were made with thermally evaporated $MAPbI_3$ in the same deposition, ensuring that the composition, thickness, and conditions are the same for each device. There was no post-deposition annealing of the thin films. This allows us to systematically attribute the causes of the difference between the *J–V* characteristics of each device architecture. Type $C_{50\ nm}$ and Type E have a thin 50 nm layer of PCBM, whereas type $C_{100\ nm}$ has a thick 100 nm PCBM layer. Schematics of the devices can be found in Figure S1 (Supporting Information).

layer of PCBM on top of c-TiO_2 as ETL, show minimal hysteresis. Finally, the inverted device (type D) shows no observable hysteresis with again the SPO being representative of the PCE. This is in good agreement with previous results, where inverted devices employing evaporated $MAPbI_3$ thin films show no hysteresis.[19]

The improved SPO after changing the ETL from c-TiO_2 (type A) to C_{60} (type B) is consistent with C_{60} being a more effective electron extraction material.[30] Furthermore the hysteresis observed in the type B devices, can be attributed to formation of pinholes in the spin coated C_{60} thin films, due to its low solubility in solvents.[31] In the pinhole regions of type B devices the $MAPbI_3$ makes direct contact with the transparent electrode, flourine doped tin oxide (FTO), as shown in Figure S8 in the Supporting Information. We have shown previously that devices with FTO/$MAPbI_3$ interfaces exhibit severe hysteresis and poor SPO.[3] The good SPO and J_{mpp} for type B devices can thus be attributed to steady-state photocurrent being shunted around these pinhole regions. However, to achieve devices with both high SPO and low *J–V* hysteresis it is important to ensure that $MAPbI_3$ does not make direct contact with the FTO.

The statistics of SPO and J_{mpp} for all devices of the four architectures are shown in Figure 1b,c, respectively. The spread in stabilized efficiencies can be attributed to both batch-to-batch variations, as a result of the deposition optimization process, and also to variations in the quality of the spin coated ETLs and HTLs. Further details of the comparison between the SPO of regular and inverted devices are provided in Figure S2 (Supporting Information), and evidence that the HTL, Spiro-OMeTAD, does not contribute to the drop in the SPO is also presented in Figure S2 (Supporting Information). Thus by assessing such a large number of devices, we can confidently attribute the discrepancy that arise between the PCE and SPO in $MAPbI_3$ planar heterojunction solar cells to the choice of the ETL.

Having established that device SPO is affected by the ETL and its charge extraction efficiency, we now discuss the origins of the hysteresis effect. To achieve this, we investigated a set of devices with different ETLs in which the $MAPbI_3$ layer was deposited in the same deposition run. This enables us to study the interface and its effect on the perovskite independent of the perovskite composition or batch variations. **Figure 2** presents a single batch of devices with identical perovskite layers and with differing ETLs, enabling us directly to compare the effect of different charge extraction layers. The specific ETL for each device was, c-TiO_2 for type A; both c-TiO_2 and a 50 nm layer of PCBM for type $C_{50\ nm}$; both c-TiO_2 and a 100 nm layer of PCBM for type $C_{100\ nm}$; and only a 50 nm layer of PCBM for type E. Figure 2a shows a cross-sectional scanning electron microscopy (SEM) micrograph of a type A device, where only c-TiO_2 is employed as an ETL. It reveals that the interface between c-TiO_2 and $MAPbI_3$ is poor with substantial low electron density (dark) regions. As will be discussed later, these low electron density regions are in fact regions of amorphous $MAPbI_3$ that result from a lattice mismatch between perovskite $MAPbI_3$ and FTO/c-TiO_2 layers. The amorphous $MAPbI_3$ at the interface leads to poor charge

collection efficiency, extensive charge recombination, and is likely to result in device hysteresis via an electrical capacitive effect across the amorphous region.[32,33]

In contrast, with the introduction of a 50 nm layer of PCBM in between the c-TiO_2 and $MAPbI_3$ (type $C_{50\ nm}$), as has been previously employed in solution-processed perovskite solar cells,[34,35] there is a considerably improved interface between the $MAPbI_3$ and PCBM as shown in Figure 2b. However, the coverage of PCBM over the rough c-TiO_2 surface is not complete, hence regions of direct contact between the c-TiO_2 and $MAPbI_3$ exist. Consequently, the *J–V* characteristics show some hysteresis even though the SPO is representative of the PCE. As shown before in Figure 2a, c-TiO_2/$MAPbI_3$ is not an ideal ETL for the $MAPbI_3$.

Doubling the thickness of the PCBM layer to 100 nm creates a pinhole-free layer which eliminates any regions of amorphous $MAPbI_3$ resulting from direct contact between $MAPbI_3$ and TiO_2. Hence an excellent interface is created for efficient electron extraction, and thus negligible hysteresis is observed (Figure 2c). Since the PCBM is deposited before the $MAPbI_3$, and there was no post-deposition annealing of these devices, it is unlikely that PCBM infiltrates between the grains. This indicates that the reduction in hysteresis, caused by PCBM, is a result of modifying the interface, rather than passivation of grain boundaries throughout the bulk. Therefore, to suppress hysteresis the ETL/$MAPbI_3$ interface incorporates an efficient electron extraction material that is free of pinholes. The features are exemplified in the type $C_{100\ nm}$ devices, while the 100 nm PCBM film is uniform and pinhole free, it is too thick to enable efficient device operation. This is evident by its considerably lower J_{sc}. As shown in type E devices, where there is only a thin layer of PCBM, there are areas at the interface where the perovskite makes direct contact with the FTO (Figure 2d). This is not ideal, as shown earlier with C_{60}, and casues *J–V* hysteresis. Other studies have shown that the optimum PCBM thickness is around 10 nm.[19] The reason why PCBM needs to be so thin is not clear, since its electron mobility is at least as high as the hole mobility in Spiro-OMeTAD. It is likely however that it requires n-type doping in order to operate efficiently at thicknesses >10 nm.

Markedly, while the reverse sweep *J–V* characteristics may not always represent the performance of the device under load, it always shows the potential of the device PCE and more specifically the $MAPbI_3$ thin film. Simply inserting a PCBM layer in the type A device to create a type $C_{50\ nm}$ device is a clear example of this. The type A devices show a reverse scan PCE of 10% and SPO of 2.7% (Table S2, Supporting Information). On the other hand, type $C_{50\ nm}$ shows an improved SPO of 12.4%, which closely represents the reverse sweep of the type A device. This is essential for troubleshooting the cause of low SPO and hysteresis observed in many perovskite devices. Modification of the interface rather than the perovskite itself should achieve a hysteresis-free device with an SPO representative of the PCE.

To gain a better understanding of the effect of the ETL on the morphology, composition, and crystal structure of the $MAPbI_3$ layer we performed TEM, high angle annular dark field (HAADF) imaging in STEM mode, and energy dispersive X-ray spectroscopy (EDX) on the type A and type $C_{100\ nm}$ devices. HAADF imaging is especially sensitive to atomic number (*Z*) contrast because heavier elements will scatter electrons at the high angles subtended by the HAADF detector. Consequently, bright regions will result from higher *Z* elements and in addition to denser regions while dark regions correspond to light elements and low density regions. The cross-sectional view of these devices reveals clear differences in the ETL/$MAPbI_3$ interface and the crystallinity of the perovskite layer. **Figure 3** a,e shows HAADF images of the type A and $C_{100\ nm}$ devices, respectively. The main difference between the two is a dark contrast region between the $MAPbI_3$ and the FTO/c-TiO_2 layers in the $C_{100\ nm}$. EDX maps of the corresponding HAADF regions are shown in Figure 3b,f with a composite false color image of the elements Pb (green), C (red), and Sn (blue). The presence of Ti from the thin layer of c-TiO_2 is shown in Figure S3 (Supporting Information). In the case of the type $C_{100\ nm}$ (Figure 3e), the darker contrast observed in the HAADF image at the interface between the FTO and $MAPbI_3$ layers corresponds to a C rich layer, observed in the EDX map, which represents the continuous conformal PCBM layer (Figure 3f). TEM analysis of the whole sample reveals that in the case of the type A devices, there was variability in the crystallinity of the perovskite layer. Electron diffraction analysis of the perovskite layers shows diffuse ring patterns of the perovskite grain that clearly illustrates the presence of amorphous regions of $MAPbI_3$ within the perovskite layer (Figure 3d). This is further supported by the high-resolution transmission electron microscopy (HRTEM) image of the type A interface which shows some amorphous $MAPbI_3$ regions (Figure 3c, light contrast). In this HRTEM image the amorphous $MAPbI_3$ can also be seen to propagate away from the TiO_2 interface, deeper into the perovskite thin film. Conversely, the type $C_{100\ nm}$ devices show a more homogeneous nucleation (Figure 3g). Electron diffraction of the perovskite layers is consistent with a higher crystallinity as shown by the selected area diffraction patterns in Figure 3h. Furthermore, the HRTEM image of the interface (Figure 3g) clearly shows the high crystallinity of the perovskite layer and the FTO/c-TiO_2 layer interlaced with amorphous regions of the PCBM. Overall, the observation of amorphous $MAPbI_3$ when in contact with FTO/c-TiO_2 provides strong evidence for the origin of hysteresis and poor SPO observed in type A devices. It is also clear that with the presence of a conformal PCBM layer with good electrical contact to a high quality perovskite layer, there is little to no hysteresis with a high SPO, as shown by the type $C_{100\ nm}$ devices. Furthermore, measurements from thermal admittance spectroscopy, suggest that the introduction of amorphous $MAPbI_3$ in combination of using TiO_2 as an ETL lead to an increase in trap density of states (Figure S4, Supporting Information). While hysteresis observed in perovskites based devices has been previously shown to be a combination of ion migration and the presence of interfacial trap states,[3,6,8,36,37] it is clear from this particular study that interface morphology of the perovskite plays a significant role in *J–V* hysteresis.

In conclusion, we have used an important advantage of the vapor deposition technique, whereupon a single batch of perovskite thin films have the same stoichiometry and thickness, to probe which particular interface is the cause of the hysteresis and deficient SPO. The results show that the quality of the interface between ETL and $MAPbI_3$, and the choice of ETL, is critical in suppressing hysteresis and reduced SPO. We observe amorphous regions of $MAPbI_3$ near the ETL

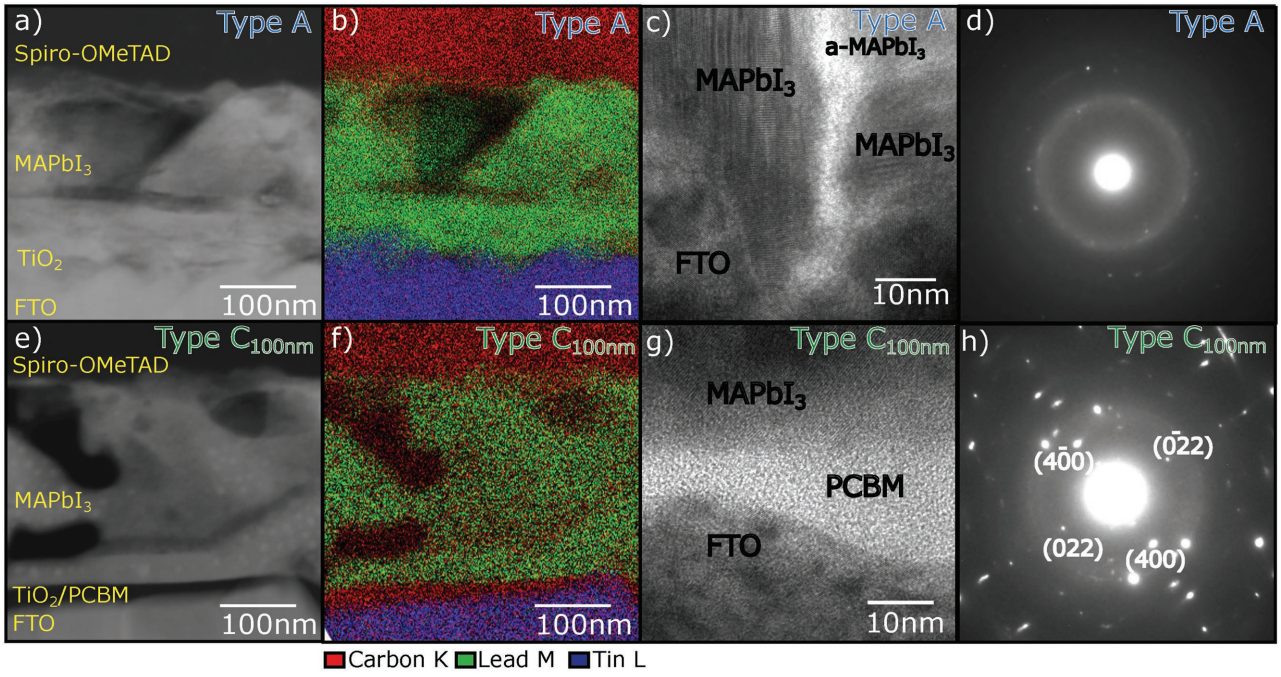

Figure 3. a) HAADF image of a type A device. b) A composite EDX map of the type A interface with carbon (red), lead (green), and tin (blue). c) HRTEM image of the interface in type A devices with amorphous perovskite labeled a-$MAPbI_3$. d) Electron diffraction pattern of the perovskite grain. e) HAADF image of a type $C_{100\ nm}$ device. f) A composite EDX map of the type $C_{100\ nm}$ interface with carbon (red), lead (green), and tin (blue). g) HRTEM of the interface in a type $C_{100\ nm}$ device. h) Electron diffraction pattern from the perovskite crystalline region (bright diffraction spots from crystalline regions). The presence of Ti from the thin layer of c-TiO_2 is shown in Figure S3 (Supporting Information).

interfaces of hysteretic devices with low SPO. We hypothesize that the poor electrical properties of the corresponding interface are a significant contributing factor affecting the device hysteresis. Therefore, the key to eliminating hysteresis from $MAPbI_3$ planar heterojunction solar cells is to develop a well-engineered interface between the perovskite layer and the (n-type) ETL. Ideally, the ETL should be an efficient electron extraction material with no pinholes, while the $MAPbI_3$ at the interface should be both homogenous and crystalline, such hysteresis-free devices have stabilized power outputs matching the power conversion efficiencies from single sweep *J–V* measurements, and are promising for large-area renewable energy generation.

Experimental Section

Device Fabrication: Fluorine doped tin oxide coated glass substrates were first cleaned with Hellmanex, acetone, isopropanol, and ozone treatment. Different transport layers were then spin coated on to substrates. This was followed by coevaporation of PbI_2 and CH_3NH_3I under high vacuum (1×10^{-6} mbar). Post-deposition annealing times varied with different devices types except for the batch studies, where there was no post-deposition annealing. Transport materials were then spin coated on top of the $CH_3NH_3PbI_3$ ($MAPbI_3$) thin film. Silver electrodes were then thermally evaporated at (1×10^{-6} mbar) with a mask to create a device with a total active area of 0.0919 cm^2. Full details of techniques and materials used to create the different device architectures are provided in the Supporting Information.

Current–Voltage Characterization: The solar cells were measured under simulated AM1.5, 100 mW cm^{-2} sunlight (1 sun), using an ABET Technologies Sun 2000 and a Keithley 2400 Sourcemeter in ambient conditions. The active area of each device was defined by a mask which exposed a 0.0919 cm^2 active area for testing of both the current voltage characteristics and stabilized power output. The devices were prebiased at 1.4 V for 5 s before initiating the reverse and forward scans. The scan rate was 0.38 V s^{-1}. Immediately after the *J–V* measurements, the SPO was measured without prebiasing. The devices were kept at the voltage defined at maximum power, which was determined from the *J–V* scans, for 50 s to measure the stabilized PCE and current density.

Scanning Electron Microscopy: Devices were sputter coated with a 3 nm conductive layer of Pt. Images were taken using a Hitachi S-4300 microscope.

Transmission Electron Microscopy: TEM samples devices were sub-100 nm thick lamella prepared by focused ion beam (FIB) using a Ga beam in an FEI Helios 600 NanoLab instrument. These samples were transferred onto a TEM carbon grid. TEM analysis was carried out in a JEOL2100F instrument operated at 200 keV and equipped with STEM capabilities and a silicon drift detector for EDX analysis.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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